

Docket No. AUS920010610US1

ABSTRACT OF THE DISCLOSURE

HARDWARE VALIDATION THROUGH BINARY DECISION DIAGRAMS INCLUDING FUNCTIONS AND EQUALITIES

5 A method, computer program product, and data
processing system for validating a hardware design using
Binary Decision Diagrams (BDDs) containing equalities and
10 function symbols is disclosed. A hardware design is
modeled in the logic of uninterpreted functions and an
expression is created that represents an equality between
an expression representing a state of the modeled design
and another expression representing the desired state of
15 the design. The equality is if-lifted to produce an
expression representing a BDD. An ordering relation
allowing atomic terms and function symbols to be compared
is established. This ordering relation is used to
repeatedly and exhaustively apply a series of
20 transformation rules to the BDD. If and only if the BDD
represents a tautology (i.e., the design is correct),
only a single node representing a "true" value will
remain.